Amendments to the Specification:

Please replace paragraph [0022] with the following amended paragraph:

[0022] The frequency estimator block (FEB) 31 of the start-up AFC comprises a Sequence Locator and Splitter 32, frequency estimators 34-38, a proportional plus integral (PI) filter 42, and a voltage controlled oscillator (VCO) or numeric controlled oscillator (NCO) 46 coupled to PI filter 42 through the sign flop 44. The input 32a to the Sequence Locator and Splitter 32 includes the PSC peak location chip-offset provided by Step 1. Start up [[AGC]] AFC 30 is an open loop gain control block that steps through pre-defined gain levels in order to set proper input power level before digitizing the input. The main input to both Step 1 and the Sequence Locator and Splitter 32 is sampled at twice the chip rate with a length of 76,800 complex elements. Since the chip-offset points to the peak location, the beginning of the PSC is 511 samples before the chip-offset. The outputs of the Sequence Locator and Splitter 32 are generated by the following general equation:

$$Output = input[i-511]\,i \qquad Eq.(1)$$